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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/749,020	12/29/2003	Cesare Clementi	61181-00010USPX	8433

23932 7590 02/13/2006

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EXAMINER	
CHEN, ERIC BRICE	
ART UNIT	**PAPER NUMBER**
1765	

DATE MAILED: 02/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/749,020	CLEMENTI ET AL.	
	Examiner	Art Unit	
	Eric B. Chen	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 14-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15-19,21-27 and 29* is/are rejected.

7)☒ Claim(s) *1-8,14,15,20,22,25 and 28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 1, 14, 15, 22, and 25 are objected to because of the following informalities: it is recommended that the phrase "substantially" be deleted (in the context of "*substantially* the same planar level" or "*substantially* the same level"). The language "substantially" is a broad term and considered relative terminology. See MPEP § 2173.05(b)(D). Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 15-17 and 21-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang (U.S. Patent No. 5,998,287), in view of Wolf, *Silicon Processing for the VLSI Era*, Vol. 4, Lattice Press (2002).

5. As to claim 15, Huang discloses a semiconductor fabrication method (column 1, lines 7-9), comprising: forming a plurality of first stripes (52) (column 2, lines 63-65) over an insulated (column 2, lines 45-48) base polysilicon layer (44) (column 2, lines 49-53) and which lie above first alternating active areas (70) (Figure 4); forming sidewall spacers (56/60) for the plurality of first stripes (52) (column 3, lines 6-8, lines 18-20; Figure 5); forming a plurality of second stripes (62) between the sidewall spacers over the insulated base polysilicon layer (44) which lie above second alternating active areas (column 3, lines 25-28; Figure 7); and removing the sidewall spacers (60) (column 3, lines 39-40).

6. Huang does not expressly disclose chemically mechanically polishing the first stripes, second stripes and sidewall spacers to substantially the same planar level. However, Huang discloses planar etching the first stripes (52), second stripes (62) and sidewall spacers (60) to substantially the same planar level (column 3, lines 25-28; Figure 8). Wolf teaches that for submicron device fabrication, a high degree of global planarization is required for both conductive and dielectric materials, achievable through the chemical mechanical polishing (CMP) technique (pages 322-23). CMP is also a well-established and well known planarization technology (pages 333-35) that makes it possible to achieve high manufacturing yields (page 324). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to

chemically mechanically polish the first stripes, second stripes and sidewall spacers to substantially the same planar level. One who is skilled in the art would be motivated to use a well-established and well known planarization technology to achieve global planarization and increase manufacturing yields.

7. As to claim 16, Huang discloses forming the plurality of first stripes (52) comprises: depositing a first material layer (column 2, lines 54-56); defining the first stripes (52) in the first material layer using a photolithography mask (column 2, lines 63-65); etching using the mask to remove the first material layer but leave the first stripes (column 2, lines 63-65; Figure 4).

8. As to claim 17, Huang discloses forming the plurality of second stripes comprises: depositing a second material layer (62) that covers the first stripes (52) and fills a region between sidewall spacers (60) (column 3, lines 25-28; Figure 7).

9. As to claim 21, Huang discloses that the first (column 2, lines 54-59) and second stripes (column 3, lines 27-29) are formed from oxide material.

10. As to claim 22, Huang discloses a method for semiconductor fabrication on a substrate including a plurality of active areas (70) (Figure 4), comprising: forming a plurality of first stripes (52) by photolithographic techniques (column 2, lines 63-65) over an insulated (column 2, lines 45-48) base polysilicon layer (44) (column 2, lines 49-53) and which lie above even ones of the plurality of active areas (70) (Figure 4); and forming a plurality of second stripes (66) without the use of photolithographic techniques (column 3, lines 25-28) over the (column 2, lines 45-48) insulated base polysilicon layer (44) and which lie above odd ones of the plurality of active areas (70) (Figure 4).

11. Huang does not expressly disclose that the plurality of first and second stripes have a polished upper surface at substantially the same planar level. However, Huang discloses that the plurality of first (52) and second stripes (62) are planar etched to substantially the same planar level (column 3, lines 25-28; Figure 8). Wolf teaches that for submicron device fabrication, a high degree of global planarization is required for both conductive and dielectric materials, achievable through the chemical mechanical polishing (CMP) technique (pages 322-23). CMP is also a well-established and well known planarization technology (pages 333-35) that makes it possible to achieve high manufacturing yields (page 324). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to polish the first and second stripes to have a polished upper surface at substantially the same planar level. One who is skilled in the art would be motivated to use a well-established and well known planarization technology to achieve global planarization and increase manufacturing yields.

12. As to claim 23, Huang discloses forming the plurality of first stripes (52) comprises: depositing a first material layer (column 2, lines 54-56); defining the first stripes (52) in the first material layer using a photolithography mask (column 2, lines 63-65); etching using the mask to remove the first material layer but leave the first stripes (column 2, lines 63-65; Figure 4).

13. As to claim 24, Huang discloses that forming the plurality of second stripes comprises: forming sidewall spacers (56/60) for the plurality of first stripes (52) (column 3, lines 6-8, lines 18-20; Figure 5); forming a plurality of second stripes (62) between the

sidewall spacers over odd ones of the active areas (70) (Figure 4); and removing the sidewall spacers (60) (column 3, lines 39-40).

14. As to claim 25, Huang discloses that forming the plurality of second stripes comprises: forming sidewall spacers (56/60) for the plurality of first stripes (column 3, lines 6-8, lines 18-20; Figure 5); depositing a second material layer (62) that covers the first stripes (52) and fills a region between sidewall spacers (60) (column 3, lines 25-28; Figure 7).

15. Huang does not expressly disclose chemically mechanically polishing to remove the second material layer but leave the second stripes such that the first and second stripes have the polished upper surface at substantially the same level. However, Huang discloses planar etching to remove the second material layer (62) but leave the second stripes (66) such that the first (52) and second stripes (66) have the upper surface at substantially the same level (column 3, lines 25-29; Figure 8). Wolf teaches that for submicron device fabrication, a high degree of global planarization is required for both conductive and dielectric materials, achievable through the chemical mechanical polishing (CMP) technique (pages 322-23). CMP is also a well-established and well known planarization technology (pages 333-35) that makes it possible to achieve high manufacturing yields (page 324). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to chemically mechanically polish to remove the second material layer but leave the second stripes such that the first and second stripes have the polished upper surface at substantially the same level. One who is skilled in the art would be motivated to use a well-

established and well known planarization technology to achieve global planarization and increase manufacturing yields.

16. As to claim 29, Huang discloses that the first (column 2, lines 54-59) and second stripes (column 3, lines 27-29) are formed from oxide material.

Claim Rejections - 35 USC § 103

17. Claims 19 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang, in view of Wolf, in further view of Kerber (U.S. Patent No. 6,027,972).

18. As to claim 19 and 27, Huang discloses using the first (52) and second stripes (66) as a hard mask (column 2, lines 54-55; column 3, lines 40-48); and etching the base polysilicon layer (44) using the first (52) and second stripes (66) hard mask (column 2, lines 54-55).

19. Huang's disclosure is related to non-volatile memory devices (column 1, lines 7-9). Kerber teaches that the common components of non-volatile memory devices are source regions, drain regions, and a floating gate region (column 1, lines 28-35). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to etch to define floating gate regions in the base polysilicon layer above both the first and second alternating active areas. One who is skilled in the art would be motivated to form a common component of a non-volatile memory device.

Claim Rejections - 35 USC § 103

20. Claims 18 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang, in view of Wolf, in further view of Hsue (U.S. Patent No. 5,310,693).

21. As to claim 18, Huang discloses forming sidewall spacers comprises: depositing a layer (56) (column 3, lines 6-7; Figure 5); and patterning the layer to remove the layer above the second alternating active areas (70) (Figure 9) but leave the layer adjacent sidewalls of the first stripes (52) (column 3, lines 18-20; Figure 6).

22. Huang does not expressly disclose that the layer is nitride. However, Huang teaches that layer (56) be preferentially etched with respect to the masking stripes (52), (column 3, lines 15-18), which are oxide (column 2, lines 54-56). Hsue discloses forming sidewall spacers comprises: depositing a nitride layer (16) (column 3, lines 1-2; Figure 3); and patterning the nitride layer to remove the nitride layer but leave the nitride layer adjacent sidewalls of the first stripes (14) (column 3, lines 5-8; Figure 3). Hsue further teaches that silicon nitride has good wet etch selectivity with respect to oxide stripes (14) (column 3, lines 16-24). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a nitride layer. One who is skilled in the art would be motivate to use a sidewall material that is preferentially etched relative to the first stripe.

Response to Arguments

23. In view of Applicants' claim amendments (Listing of Claims, pages 2-10), filed Nov. 28, 2005, and the claim amendments to Clementi (Application No. 10/746,878,

Listing of Claims, pages 2-8), filed Nov. 28, 2005, provisional rejection of claims 1, 3, 15-18, and 22-26 are under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-2 and 7-15 of copending Application No. 10/746,878, Clementi, has been withdrawn. The claims for the two co-pending applications no longer conflict.

24. In view of Applicants' amendments to claim 14 (Listing of Claims, page 5), filed Nov. 28, 2005, the rejection of claim 14 under 35 U.S.C. 112, second paragraph, has been withdrawn.

25. Applicant's arguments (Applicants' Remarks, page 11), filed Nov. 28, 2005, with respect to the rejection of claim 1 under 35 U.S.C. 103(a) as being unpatentable over Kerber, in view of Kim, have been fully considered and are persuasive. The Kim reference does not teach or suggest "polishing said layer of a third material together with said alternated stripes and said spacers to... the same level." The rejection of claims 1-8 has been withdrawn.

26. Applicant's arguments (Applicants' Remarks, page 12), filed Nov. 28, 2005, with respect to the rejection of claim 14 under 35 U.S.C. 103(a) as being unpatentable over Kerber, in view of Kim, have been fully considered and are persuasive, as discussed above.

27. Applicant's arguments (Applicants' Remarks, page 13), filed Nov. 28, 2005,with respect to the rejection of claims 15-17, 19, 22-25 and 27 under 35 U.S.C. 103(a) as being unpatentable over Kim, in view of Kerber, have been fully considered and are persuasive. The Kim and Kerber references do not teach or suggest polishing the

upper surface to the same planar level. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Huang and Wolf.

28. Applicant's arguments (Applicants' Remarks, page 13), filed Nov. 28, 2005,with respect to the rejection of claims 18, 20-21, 26, and 28-29 under 35 U.S.C. 103(a) as being unpatentable over Kim, in view of Kerber, in further view of Wolf, have been fully considered and are persuasive. The Kim and Kerber references do not teach or suggest polishing the upper surface to the same planar level. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Huang and Wolf.

Allowable Subject Matter

29. Claim 1 is objected to, but would be allowable if rewritten with the term "substantially" deleted. Claims 2-8 are objected to because they depend on claim 1.

30. The following is a statement of reasons for the indication of allowable subject matter for claim 1: the prior art fails to teach or suggest polishing said layer of a third material together with said alternated stripes and said spacers to the same planar level. The closest prior art, Kim, discloses an etch back technique for stripes (4/6), producing a rougher surface (column 2, lines 37-44; Figure 1B). Similarly, Hsue (U.S. Patent No. 5,310,693) discloses stripes (18/14) with sidewall spacers (16) (Figures 4-5) with no planarization of stripes (18/14). However, there is no motivation or suggestion of

polishing said layer of a third material together with said alternated stripes and said spacers to the same planar level, as in the context of claim 1.

31. Claim 14 is objected to, but would be allowable if rewritten with the term "substantially" deleted.

32. The following is a statement of reasons for the indication of allowable subject matter for claim 14: the prior art fails to teach or suggest polishing the stripes and spacers to the same planar level, as discussed above.

33. Claim 20 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims and if rewritten with the term "substantially" deleted from claim 15.

34. The following is a statement of reasons for the indication of allowable subject matter for claim 20: the prior art fails to teach or suggest that the first and second stripes are formed from polysilicon material. The closest prior art, Huang, discloses the first (52) and second stripes (62) as either an oxide or nitride masking material (column 2, lines 54-58; column 3, lines 25-28). Moreover, Wolf et al., *Silicon Processing for the VLSI Era*, Vol. 1, Lattice Press (1986) teaches that polysilicon is widely used for electrodes and interconnections (page 175). However, there is no suggestion or motivation that the first and second stripes are formed from polysilicon material, as in the context of claim 20.

35. Claim 28 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the

base claim and any intervening claims and if rewritten with the term "substantially" deleted from claim 22.

36. The following is a statement of reasons for the indication of allowable subject matter for claim 28: the prior art fails to teach or suggest that the first and second stripes are formed from polysilicon material, as discussed above.

Conclusion

37. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric B. Chen whose telephone number is (571) 272-

2947. The examiner can normally be reached on Monday through Friday, 8AM to 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine G. Norton can be reached on (571) 272-1465. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EBC EBC
Jan. 20, 2006

NADINE G. NORTON
SUPERVISORY PATENT EXAMINER